CNTFET based Highly Durable Radix-4 Multiplier using an Efficient Hybrid Adder

N. Mathan

Assistant Professor,Department of ECE, Sathyabama University, Chennai, India.

CNTFET is a novel device that is projected to outperform scaled CMOS technologies.Multiplier is one of the very important hardware blocks such as FIR filters, digital signal processors etc.The performance speed of the multiplier often affects the overall speed performance in VLSI systems. On the whole, multiplication employs most of the execution time in many Digital signal processor (DSP) devices. So, high speed multiplier is greatly desired. In this paper, a high speed existing radix-4 multiplier based Shannon adder is analysed intensively. To achieve an efficient radix-4 multiplier, the proposed hybrid adder was implemented for further power reduction in high speed parallel radix-4 multiplier circuits. The proposed radix-4 multiplier is more desirable for obtaining the low power consumption, less propagation delay and efficient power delay product. Simulations are executed using Synopsys HSpice in 32nm CMOS and 32nm CNTFET Technologies. The simulation results exhibits the transcendences of the proposed structures in terms of Power consumption, propagation delay and Power delay product compared to the advanced technology of CMOS and CNTFET based designs.

Keywords: Shannon adder, hybrid adder, CPL, radix-4 multiplier.

Multiplication is one of the most important functions in arithmetic operations. A high-speed multiplier is greatly desired, since multiplication utilizes most of the execution time in many Digital Signal Processor (DSP) devices [1]. There are three important issues to be considered in the Very Large Scale Integration (VLSI) design: the chip area, speed of computation and power dissipation [1] considering speed, the Braun multiplier, Booth multiplier and high-radix multiplier are the fastest types of multipliers [3]. Parallel multipliers carry out high-speed operations; however, there is a trade off with the large circuit area and high power consumption. Therefore, one of the most important tasks in VLSI design is to reduce the power consumption and area size whilst retaining high performance.

Addition is an important component of arithmetic operations, like subtraction, multiplication and division [4]. The proposed multiplier circuits make use of an adder cell to accomplish the multiplication algorithm, and two types of adder cells have been implemented in the multiplier circuits: namely, the half adder cell and full adder cell. Basic multiplication can be realized by the shift-add algorithm by generating partial products and adding successive properly shifted partial products. Thus, multiplication is proportional to the number of partial products to be added [5]. High radix multiplication algorithms can reduce the number of partial products by handling more than 1 bit of the multiplier in each cycle; so, fewer cycles are required as it moves to higher radices. Furthermore, the reduction of the

---

* To whom all correspondence should be addressed.
E-mail: mathanmaestro@hotmail.com

number of cycles, along with the incorporation of recoding and carry-save addition to simplify the required computations in each cycle, allow for a significant improvement in the speed of high-radix multipliers [6].

This paper proposes an adder cell that combines the 10T, Modified Shannon and Hybrid adder. The adder cells are implemented into an 8 × 8 bit high radix multiplier. The simulation results for 8 × 8 bit high radix multipliers are based on the CNTFET over Complementary Metal Oxide Semiconductor (CMOS) design rule for low-power and high-speed application. The proposed adder-based radix-4 multipliers are compared in terms of speed, area and power dissipation. The proposed hybrid adder cell-based multiplier is compared with other existing multiplier based adder circuits in terms of power consumption, propagation delay, and power delay product. Our adder-based multiplier demonstrates better performance than the other multiplier circuits for all parameters.This paper is organized as follows: In section 2, existing Shannon adder and hybrid adder are implemented in radix-4 multiplier is described. In section 3, proposed hybrid adder and proposed radix-4 multiplier is presented. In section 4, simulation results and performance analysis is given and eventually in section 5, concludes the paper.

Carbon Nanotube Field Effect Transistor(CNTFET)

Carbon Nano Tubes (CNTs) are sheets of Graphene rolled into tube [4]. Depending on their chirality (i.e., the direction in which the graphite sheet is rolled), the single-walled carbon nanotubes can either be metallic or semiconducting [5], [6]. CNFETs are one of the molecular devices that avoid most fundamental silicon transistor restriction and have ballistic or near ballistic transport in their channel [7], [8]. Therefore a semiconductor carbon nanotube is appropriate for using as channel of field effect transistors [6]. Applied voltage to the gate can control the electrical conductance of the CNT by changing electron density in the channel.

For a CNT with (n, m) as chirality and a as lattice (that is carbon to carbon atom distance) the diameter is [10]. As mentioned above, CNTs are used in CNFETs as channel and depending on the connections between source and drain with channel (CNTs) there are two main CNFETs. It works on the principle of direct tunnelling through a

Schottky barrier at the source–channel junction [11] therefore; these transistors are called Schottky Barrier CNFET (SB-CNFET). SB-CNFET shows ambipolar behavior and Constrain usage of these transistors in conventional CMOS-like logic families. Schottky barrier restricts the transconductance in the ON state, and thus Ion/Ioff ratio becomes rather low [12]. Second device is MOSFET-like CNFET which is doped in un-gated portions and has similar behaviour to CMOS transistors and it presents unipolar behaviour [13]. The semiconductor-semiconductor junction will eliminate schottky barrier and therefore there is higher ON current unlike SB-CNFETs. Other advantages of MOSFET-like CNFETs are high on-off ratio and their scalability compared to their schottky barrier counterparts [8]. In this paper we utilized MOSFET-like CNFETs for proposed design.

Previous Work

Adder is basic building block module in all multipliers. Multiplier is an important kernel of digital signal processors. So, employing low power and fast multipliers play a key role in the performance of real time applications. In this section, existing radix-4 multiplier based Shannon adder are described and analysed.

Shannon adder

The Shannon adder is designed with the Complementary Pass Transistor Logic (CPL) technique and the multiplexing control input technique (MCIT) for both sum and carry operations. The sum operation is designed based on equation(1) where two XOR logic gates are used, since pass-transistor logic is advantageous in constructing XOR logic gates. On the other hand, the carry circuit is designed with respect to equation (2). By combining the sum and carry circuits, the XOR gate in the carry operation can be omitted, and both circuits can share the common term, a xor b, in the sum operation.

Sum = A xor B xor C   .... (1)
Cout = (A xor B) Cin +AB   .... (2)

The inputs A, A's complement (A'), B, and B's complement (B') are fed as inputs to the pass transistors and form an XOR logic gate. These four inputs construct an XOR logic operation in transistor level, which is designed with two transistors. To reduce the number of transistors, the output of the XOR gate (A xor B) is fed through an NOT gate from the differential node to the pass

transistors as a control input. On the other hand, Cin is treated as variable input, which is fed through the pass transistor's source terminal. At this stage, the functionality of the circuit is equivalent to sum operation, sum A xor B xor C, and six transistors are used. As mentioned previously, the number of transistors in the carry operation can be optimized by taking A xor B as the input from the sum operation circuit AND with Cin to produce the operation equivalent to (A xor B) Cin, which only uses another two transistors. Meanwhile, the inputs A, A', B, and B' are fed in to pass transistors to produce AND logic gate, which represents the AB operation in Equation (2). The outputs of both (A xor B) Cin and AB are used as multiplexing inputs to sum both terms with the OR gate operation. The transistor count can be minimized by modifying the OR gate at the last stage of the carry equation. This is achieved by removing the inverter and transistor fed by the inverter. Markovic's full adder circuit has 22 transistors. At an earlier point, 3 transistors were omitted in this design and the number of transistors of the full adder cell was reduced to 17 as shown in Figure.2 after applying the redundant transistor reduction technique.
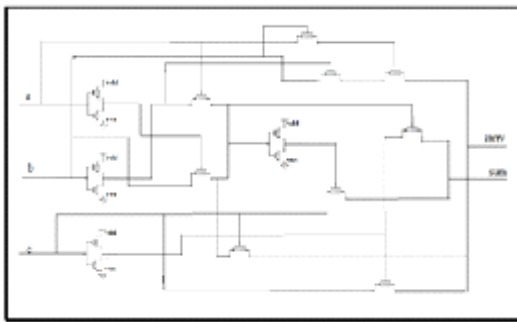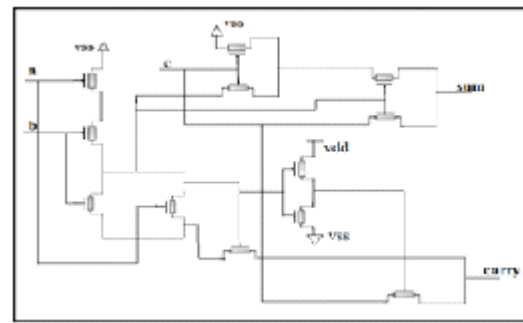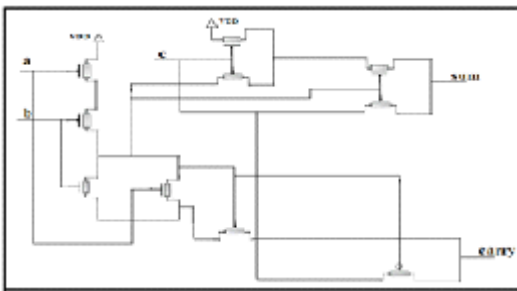
Hybrid adder

A Hybrid adder is a combination of 14T sum and modified Shannon carry. It consists of 12 transistors. The width is optimized by transistor sizing to bring the better power consumption without degrading the delay. For further improvement in terms of power, delay and driving capability Hybrid full adder circuit is implemented as shown in Figure.2. Hybrid full adder circuits provide good driving capability and better power delay performance.

Proposed Work

In this section, proposed hybrid adder and proposed radix-4 multiplier has discussed and it observed the performance.

Proposed Hybrid Adder

A Hybrid adder is proposed by modifying the existing hybrid adder. In existing system, inverter is used in the design; the modified design doesn't consist of inverters since they are Power hungry components. The nMOS transistor that needs the inverted input has been replaced by pMOS transistor as shown in Figure.3. Hence, overall area, power consumption and switching activities are reduced in which the design becomes prominent for low power applications.

Fig. 1. Shannon adder[9]

Fig. 2. Hybrid adder
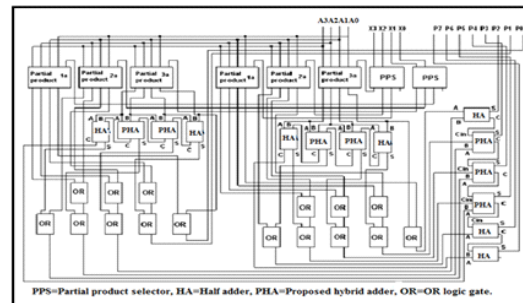

Fig. 3. Proposed Hybrid adder

Fig. 4. Highly Durable Radix-4 multiplier using proposed Hybrid adder

Architecture of Proposed Radix-4 Multiplier

      Parallel multipliers carry out high speed operations. However, there is tradeoff with large circuit area and high power consumption. In radix-4 multiplier full adder has been chosen in order to reduce the power consumption. Finally, the
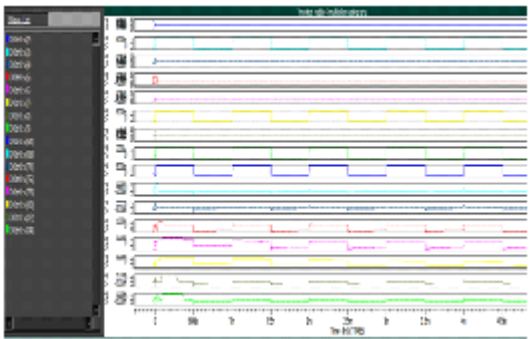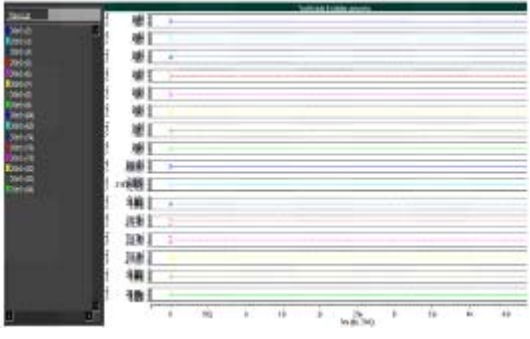

Fig. 5. Radix-4 multiplier based Shannon adder output

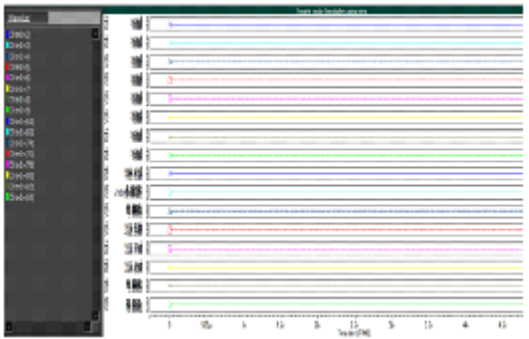**Fig. 6.** Radix-4 multiplier based hybrid adder output

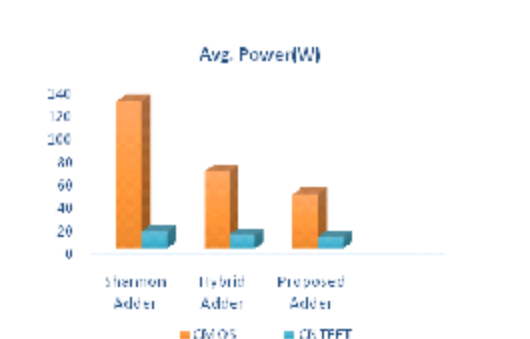**Fig. 7.** Radix-4 multiplier based proposed hybrid adder

Fig. 8. Performance Analysis of Radix-4 multiplier using Average Power

Table. 1. Comparison of Radix-4 Multiplier using existing and proposed adder in 32nm using CMOS Technology.

RADIX-4MULTIPLIER	CMOS DESIGN 32nm		
	AVG. POWER(W)	DELAY(s)	PDP(J)
SHANNON ADDER	1.28e-4	73.9e-12	9.5e-15
HYBRID ADDER	6.75e-5	46.8e-12	3.16e-15
PROPOSED HYBRID ADDER	4.79e-5	20.5e-12	9.8e-16

Table. 2. Comparison of Radix-4 Multiplier using existing and proposed adder in 32nm using CNTFET Technology

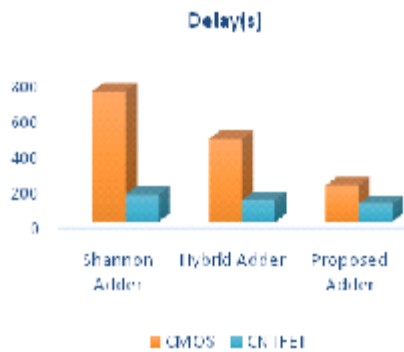| RADIX-4MULTIPLIER	CNTFET DESIGN 32nm		
	AVG. POWER(W)	DELAY(s)	PDP(J)
SHANNON ADDER	1.55e-7	158.9e-15	2.46e-20
HYBRID ADDER	1.26e-7	35.3e-16	4.45e-22
PROPOSED HYBRID ADDER	1.02e-7	32.6e-16	3.33e-22

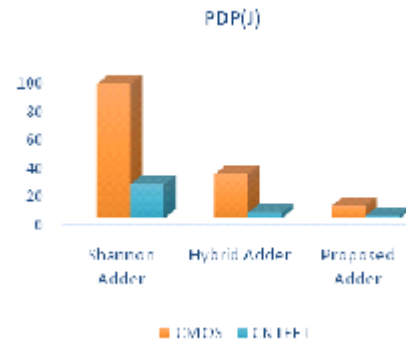**Fig. 9.** Performance Analysis of Radix-4 multiplier using Delay

Fig. 10. Performance Analysis of Radix-4 multiplier using PDP

proposed Hybrid adder based radix-4 multiplier is compared with existing adder based multiplier in terms of power, delay and power delay product. Our proposed adder based multiplier circuits as shown in Figure.4 may be used in high-speed application circuits due to its less propagation delay.

RESULTS AND DISCUSSION

Transient analysis

To evaluate the performance of Shannon adder, hybrid adder and proposed hybrid adder circuits. Then existing and proposed adder based Radix-4 multiplier circuits discussed in this paper are designed in 32nm CNTFET over the CMOS Technology. All simulations are performed in HSpice simulation tool. Figure's 5, 6 and 7 represent the simulation results of the above mentioned circuits.

Figure-5 describes the transient analysis of Existing Radix-4 Multiplier using Shannon Adder output where V(2,3,4,5,6,7,8,9) represents the inputs and V(64,65,74,76,78,80,82,84) represents the output.

Figure-6 describes the transient analysis of Existing Radix-4 Multiplier using hybrid Adder output where V(2,3,4,5,6,7,8,9) represents the inputs and V(64,65,74,76,78,80,82,84) represents the output.

Figure-7 describes the transient analysis of Radix-4 Multiplier using proposed hybrid Adder

output where V(2,3,4,5,6,7,8,9) represents the inputs and V(64,65,74,76,78,80,82,84) represents the output.

Performance analysis

Table.1 and 2 represents Comparison of Radix-4 Multiplier using existing and proposed adder in 32nm using both Technology.

Comparing the power, delay and power delay product of proposed Radix-4 multiplier using Modified Hybrid Adder design is efficient than the existing adder by using both technology as shown in Table 1 and Table 2.

Figure 10 represents the performance analysis chart of Radix-4 multiplier using power delay product.

CONCLUSION

The parallel multipliers are much option than the serial multiplier in terms of Power consumption and Area. In this paper, Hybrid full adder is proposed and it is implemented in radix-4 multiplier. The existing radix-4multiplier based Shannon adder, hybrid adder and proposed radix-4 multiplier based hybrid adder are simulated using HSpice in 32nm CNTFET over the CMOS Technology. The power, delay and power delay product values of all designs are analysed. It is noted that, while comparing the existing radix-4multiplier based Shannon adder and hybrid adder the proposed radix-4 multiplier consumes lowest delay, lesser power consumption and reduced

power delay product is good and it gives better performance. Then the proposed circuit gives speed up the calculation. Also, it reduces the number of partial product and thus has the potential of power saving which can be used for low power application.

ACKNOWLEDGEMENT

The author of this work is extremely grateful to Honourable Chancellor Colonel Dr.Jeppiaar, Sathyabama University, Dr.Marie Johnson and Dr.Mariazeena Johnson, Directors, Dr. B.Sheela Rani, Vice-Chancellor, Dr.T.Sasipraba, Dean, (Publications & Conferences), Dr. P.E.Sankaranarayanan, Dean (Academic Research), Dr.S.S.Rau, Registrar and Dr.K.V.Narayanan, Controller of Examinations, Sathyabama University for their constant support and motivation extended to them during the course of the research.

REFERENCES

1. Costa.E, Bambi.S, and José Monteiro "A New Architecture for Signed Radix-2Pure Array Multipliers" Proceedings of the 2002 IEEEInternational Conference on Computer Design: VLSI in Computersand Processors (ICCD.02).
2. Markovic. D, B. Nikolic, V.G. Oklobdz (2000), "A general method in synthesis of pass-transistor circuits," Microelectronics Journal 31, pp-991-998
3. Park.B, Shin.M, Park.I.C, and Kyung.C.M, "Radix-4 multiplier with regular layout structure," Electronics Letter, vol. 34, no. 15, pp.1446-7, 1998.
4. Parhami,B "Computer Arithmetic algorithms and Hardware Designs," Oxford University Press 2000. ISBN 0-19-512583-5.
5. Psilogeorgopoulos.M, Munteanu.M, Chuang.T.S, Ivey.P.A, and Seed.L "Contemporary Techniques for Lower Power Circuit Design," PRESTDeliverable D2.1 version 0.1, 2000.
6. Sathiyabama., Raja Shailaja (2012) "A Survey of Low Power High Speed Full Adder", International Journal of Emerging Technology and Advanced Engineering (IJETAE), ISSN 2250-2459, Volume 2, Issue 9, pp.527 -532.
7. Sathiyabama.B, Malarkkan.S "Novel Low Power Hybrid Adders Using 90nm Technology for DSP Applications" International Journal of Engineering Research and Development, ISSN: 2278-067X, volume 1, issue 2 (May 2012), pp.29-33.
8. Senthilpari.C, Ajay Kumar Singh, Diwakar.K "Design of a low-power, high performance, 8× 8bit multiplier using a Shannon-based adder cell", *Microelectronics Journal,* 2008; **39**, issue- 5, pp.812-821.
9. Senthilpari.C "A Low power and High performance radix – 4 multiplier design using a modified Pass Transistor logic Technique" *IETE Journal of Research,* 2011; **57**(2), pp.149 -155.
10. Yamanaka.Y.K, Nishida.T, Saito.T, Shimohigashi.M, and Shimizu.K, Hitachi Ltd., Tokyo "A 3.8-ns CMOS 16×16-b multiplier using complementary pass-transistor logic," *IEEE Journal of Solid-StateCircuits,* 1990; **25**(2), pp. 388-95.
11. Yeo.K and Roy.K "Low-voltage, low power VLSI sub system" Mc Graw-Hill publishcation, 1998.
12. Oscal.T, Chen.C, Wang.S, and Y W Wu, "Minimization of Switching Activities of Partial Products for Designing Low-PowerMultipliers, IEEE Transaction on Very Large Scale Integration (VLSI) Systems, 2008; **11**(3), pp. 418-33.